

**REMARKS**

Claim 7 has been modified to clarify the invention and better define the invention over the prior art. Specifically, the features of claims 8 and 9 have been incorporated into independent claim 7 and claims 8 and 9 have been cancelled. And, claim 10 has been rewritten in independent form. No new matter has been added by the aforementioned changes.

The allowance of claims 1-6 is noted, with thanks.

Turning to the art rejections, claim 8 has been canceled, thus rendering moot the rejection of that claim. As to the rejection of claims 7 and 11 under 35 USC 102(b) as being anticipated by Sasaki (US Patent No. 6,064,118) as noted, *supra*, claim 7 has been amended to incorporate the limitations of claims 8 and 9. Thus, independent claim 7, as amended, requires the step of "forming an interlayer insulating film over the entire surface of said semiconductor substrate after the step of forming said second trench, wherein said step of forming an interlayer insulating film comprises forming a cavity within said second trench." Neither Sasaki nor Yamada et al. teach forming an interlayer insulating film as required by claim 7. Thus, claim 7 and claim 11, which depends therefrom, cannot be said to be anticipated by or for that matter obvious from Sasaki alone or taken with Yamada et al.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

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Respectfully submitted,



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